IN THE CLAIMS

1. (Canceled)

2. (Canceled)

3. (Canceled)

4. (New) A method of processing digital input data to produce different digital output data using a processing circuit comprising flip flops each comprising a first latch and a second latch coupled in series, the method comprising:

Rule 126 providing first and second non-overlapping clock signals;

computing said digital output data, comprising:

clocking first latches of said flip flops using said first non-overlapping clock signal; and

clocking second latches of said flip flops using said second non-overlapping clock signal; and

outputting said digital output data.

5. (New) The method of claim 4, further comprising:

producing multiple successively-delayed versions of the first clock signal;

producing multiple successively-delayed versions of the second clock signal;

clocking different subsets of the first latches using different respective ones of the successively-delayed versions of the first clock signal; and

clocking different subsets of the second latches using different respective ones of

Rule 126 the successively-delayed versions of the second clock signal.

6.

~~4.~~ (New) Circuitry for processing digital input data to produce different digital output data, comprising:

first and second non-overlapping clock signals;

means for computing said digital output data, comprising flip flops each comprising:

a first latch of said flip flops, clocked using said first non-overlapping clock signal; and

a second latch of said flip flops, clocked using said second non-overlapping clock signal, wherein said first latches and said second latches are coupled in series.

7.

~~5.~~ (New) The circuitry of claim 4, further comprising:

means for producing multiple successively-delayed versions of the first clock signal;

means for producing multiple successively-delayed versions of the second clock signal; and

a clock network wherein:

different subsets of the first latches are clocked using different respective ones of the successively-delayed versions of the first clock signal; and

different subsets of the second latches are clocked using different respective ones of the successively-delayed versions of the second clock signal.